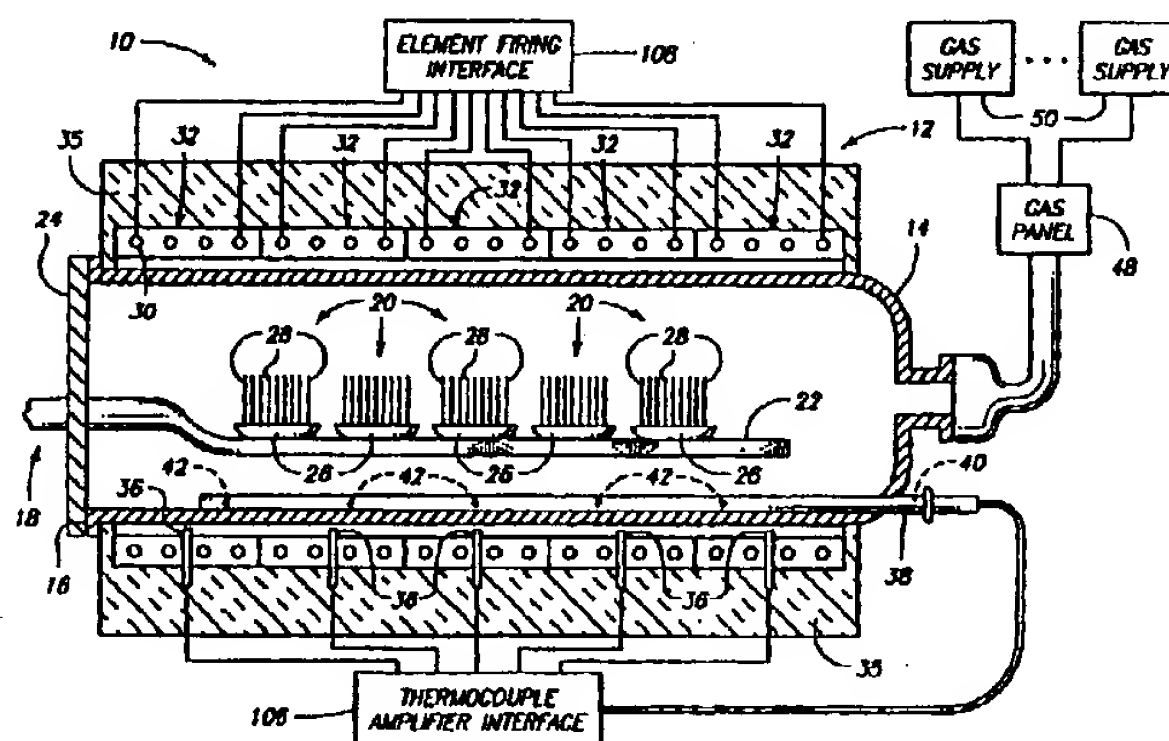




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<p>(21) International Application Number: PCT/US98/01076 (22) International Filing Date: 27 January 1998 (27.01.98) (30) Priority Data: 08/791,024 27 January 1997 (27.01.97) US (71) Applicant: SEMITool, INC. [-/US]; 655 W. Reserve Drive, P.O. Box 7010, Kalispell, MT 59901 (US). (72) Inventors: STODDARD, Kevin; Suite 201, 2340 W. Shangri La, Phoenix, AZ 85029 (US). HUGUES, Jean, Benoit; P.O. Box 7010, Kalispell, MT 59904 (US). TSAKALIS, Konstantinos; Suite 201, 2340 W. Shangri La, Phoenix, AZ 85029 (US). (74) Agents: POLIT, Robert, B. et al.; McAndrews, Held & Malloy, Ltd., Suite 3400, 500 West Madison Street, Chicago, IL 60661 (US).</p>	<p>(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).</p> <p>Published <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i></p>	

(54) Title: MODEL BASED TEMPERATURE CONTROLLER FOR SEMICONDUCTOR THERMAL PROCESSORS



(57) Abstract

Controllers and associated methods for controlling a thermal reactor or other thermal semiconductor processors which include a heating element (30) powered by a power source, and having profile thermocouples (42) and spike thermocouples (36). One preferred method comprises the following steps: modeling thermal dynamic characteristics of the thermal reactor (12), the modeling step including providing thermocouple instrumented wafers (26) in the thermal reactor, perturbing the thermal reactor by controlling the heating element (30) using a stimulation sequence, and developing models based on changes in temperature created by the perturbations. The models are developed off-line and can include one or more models, such as a model of power versus spike thermocouple readings, a model of spike thermocouple reading versus profile thermocouple readings, and a model of profile thermocouple readings versus thermocouple instrumented wafer readings. On-line models are further derived and used during operation to control power input to the zones of the thermal processor using measured profile and spike temperatures. The models can be cascaded or selectively activated to achieve different control regimes.

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4 **Model Based Temperature Controller For Semiconductor Thermal**
5 **Processors**
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8 **TECHNICAL FIELD**

9 The invention relates to semiconductor processing methods
10 and apparatus. More particularly, the invention relates to
11 process controllers principally for controlling temperature and
12 possibly other process variables in thermal reactors and other
13 processors used in semiconductor processing.
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17 **BACKGROUND OF THE INVENTION**

18 The processing of semiconductor wafers has become of great
19 economic significance due to the large volume of integrated
20 circuits being produced and the significant value associated
21 with such circuits. Competitive pressures have driven dramatic
22 changes in production. Foremost among these is the reduction
23 in size of the various features of an integrated circuit which
24 make up the transistors and other devices being formed on the
 integrated circuits. This reduction in feature size has been
 driven to achieve greater levels of integration, more
 sophisticated and complex circuits, and to reduce production
 costs by obtaining more integrated circuits on each wafer being
 produced.

 Even though feature sizes used in integrated circuits have
 decreased dramatically, additional reductions are continuously
 being pursued. The temperature at which wafers are processed
 has a first order effect on the diffusion of dopants,

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3 deposition of materials or other thermal processes being
4 performed. Thus it is important to have processing equipment
5 which can achieve accurate temperature control to meet desired
6 thermal processing specifications. As feature size decreases,
7 the importance of accurate temperature control during
8 processing increases to even a greater degree.
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12 Traditionally, semiconductor thermal reactors have used
13 Proportional-Integral-Derivative (PID) controllers to control
14 temperature. Although such controller have the advantage of
15 easier operation and maintenance, they are of limited accuracy
16 in controlling temperatures. This limited accuracy imposes
17 limitations on the achievable size and yield of integrated
18 circuits.
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21 The more typical PID controller parameters are
22 experimentally tuned by adjusting the gain values or selected
23 using a variety of tuning rules (e.g., Ziegler-Nichols). Such
24 control methods give relatively less accurate control of the
temperature of the thermal reactor with associated limitations
on production yield and consistency of the resulting integrated
circuits or other semiconductor items being produced.

More complex control schemes have been devised, but these
more complex schemes frequently are so complex computationally
that on-line operation is either not possible or not feasible.

More complex control schemes have also in some cases not been
used because of difficulties in achieving required control
system tuning and maintenance at the production facility. This
has been of somewhat greater concern with regard to controllers

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3 operated by engineers who do not have strong control system
4 backgrounds. As a result is it often difficult for them to
5 resolve all of the complexities imposed in adjusting the
6 control system to the variations in their specific processor
7 performance. This is exacerbated by variations in the same
8 processor with time and changing conditions.
9
10

11 The temperature control problems encountered in thermal
12 processing of semiconductor devices can be thought of in
13 several different ways. One control problem involves matching
14 the wafer temperature to the desired overall or average target
15 or recipe temperature of the processor. The problem involves
16 both achieving the desired recipe temperature and in achieving
17 relatively consistent temperatures from one production run to
18 another.
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22 The desired overall or average recipe temperature of the
23 processor can conveniently be thought of in terms of three
24 different phases. The first phase is typically a ramp-up phase
wherein the average operating temperature increases or ramps
from a low level when processing is begun. The temperature
ramp-up phase is thereafter typically followed by a period
during which a desired maximum or other constant processing
temperature is maintained. Such a constant temperature phase
includes a stabilization period during which the changing
temperature ramp ends and a constant or near constant
temperature is achieved. Constant temperature phases may occur
one or more times in a processing cycle. A further phase is
the ramp-down phase wherein the average temperature of the

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3 processor in decreasing. Appreciate that various processes may
4 include more than one of each of these three different phases.
5

6 Whether simple or more complex temperature plans or
7 recipes are used, each phase may further be complicated by the
8 introduction of one or more supplementary processing gases or
9 vapor phase processing constituents which affect temperature
10 and thermal response. Such supplementary processing gases are
11 typically gases containing dopants, deposition materials or
12 steam.
13
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15 Another temperature control problem is to achieve
16 relatively similar temperature exposures or histories during a
17 processing cycle for each of the wafers or other semiconductor
18 workpieces being processed within a batch. Temperature
19 variations routinely occur with regard to wafers positioned
20 near the ends of the array of wafers held within a processing
21 furnace. There may also be other less predictable variations
22 from wafer to wafer, such as along the array of wafers
23 contained within the processing array.
24

A still further temperature control problem is associated
with temperature variations across an individual wafer or other
semiconductor workpiece being processed. This area of
variability is exemplified by the geometry of most processing
furnaces which have a grouping of multiple electrical heating
elements formed in rings which surround the array of wafers
being processed. Heat from the heating elements is being
radiated through the processing vessel and variations can occur
with regard to the heat gain experienced by the peripheral

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3 areas of the wafer as compared to the interior areas.
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5 Variations in the degree of radiant heat transfer and radiant
6 shadowing which occur from wafer to wafer further exacerbates
7 this problem.
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9 Another noteworthy consideration is the manufacturing
10 concern to minimize the processing time used to effect a
11 particular process or group of processes being carried out with
12 the thermal processor. Minimizing the processing time will
13 typically increase the ramp-up phase temperature change rate.
14 Conversely, time concerns will also increase the ramp-down
15 phase temperature change rate. Increased rates of temperature
16 change cause greater difficulties in maintaining recipe
17 temperatures during the processes of transitioning between
18 ramp-up and stabilization phases, and between stable
19 temperatures and relatively rapid temperature ramp-down phases.
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24 Given these complexities and somewhat countervailing
considerations, there is great difficulty in achieving improved
control systems which are both practical and workable for
improved thermal processing of semiconductor wafers.

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5 **BRIEF DESCRIPTION OF THE DRAWINGS**

6 Fig. 1A is a side elevational view, partially in section,
7 of a thermal reactor system embodying the invention.
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9 Fig. 1B is a side elevational view, partially in section,
10 of the thermal reactor system of Fig. 1A during modeling and
11 characterization using thermocouple instrumented wafers.
12

13 Fig. 2 is a block diagram illustrating a preferred
14 temperature controller according to the invention.
15

16 Fig. 3 is a block diagram illustrating operation of a
17 process sequencing subsystem and gas interface.
18

19 Fig. 4 is a block diagram illustrating operation of a
20 temperature subsystem.
21

22 Fig. 5 is a waveform diagram illustrating an exemplary
23 pseudo-random binary sequence used to characterize the reactor
24 of Fig. 1A.

Fig. 6 is a control diagram of a characterization control mode which uses the pseudo-random binary sequence of Fig. 2 to characterize the reactor of Fig. 1A prior to actual use in processing semiconductor wafers.

Fig. 7 is a control diagram of an element control mode logic circuit, which employs a spike controller.

Fig. 8 is a control diagram of a base control mode logic circuit, which employs a profile controller and the spike controller of Fig. 7.

Fig. 9 is a control diagram of a dynamic control mode logic circuit, which employs a wafer controller, the profile

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3 controller of Fig. 8, and the spike controller of Fig. 7.
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5 Fig. 10 is a control diagram of a Dt control mode logic
6 circuit, which employs a Dt non-linear controller, the profile
7 controller of Fig. 8, and the spike controller of Fig. 7.
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9 Fig. 11 is a flowchart illustrating design of the
10 preferred controllers.
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5 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

6 This disclosure of the invention is submitted in
7 furtherance of the constitutional purposes of the U.S. Patent
8 Laws "to promote the progress of science and useful arts"
9 (Article 1, Section 8).
10

11 The invention provides controllers and methods for
12 controlling a thermal reactor or processor used to process
13 semiconductor workpieces. The typical thermal reactor includes
14 a heating element powered by a power source, and has profile
15 thermocouples and spike thermocouples. A preferred method
16 comprising the following steps: modeling thermal dynamic
17 characteristics of the thermal reactor, the modeling step
18 including providing thermocouple instrumented wafers in the
19 thermal reactor, perturbing the thermal reactor by controlling
20 the heating element using a stimulation sequence, and
21 developing models based on changes in temperature created by
22 the perturbations, the models including a model of power versus
23 spike thermocouple readings, a model of spike thermocouple
24 readings versus profile thermocouple readings, and a model of
profile and spike thermocouple readings versus thermocouple
instrumented wafer readings.

 One aspect of the invention provides a controller unit for
controlling a thermal reactor supporting a heating element
powered by a power source, profile thermocouples and spike
thermocouples, and selectively receiving thermocouple
instrumented wafers, the controller unit comprising an input

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3 device receiving a recipe; and a plurality of selectable
4 control mode logic circuits communicating with the profile
5 thermocouples and spike thermocouples, the control mode logic
6 circuits being used to control the heating element relative to
7 the recipe.
8
9

10 Another aspect of the invention provides a method for
11 controlling a thermal reactor including a thermal reactor
12 supporting a heating element powered by a power source, profile
13 thermocouples, and spike thermocouples, and selectively
14 receiving thermocouple instrumented wafers, the method
15 comprising the following steps: modeling thermal dynamic
16 characteristics of the thermal reactor using the profile
17 thermocouples, spike thermocouples, and instrumented wafers;
18 receiving a recipe including desired temperatures with respect
19 to time, and the recipe including desired control modes with
20 respect to time; and switching from one control mode to another
21 in accordance with the recipe, and controlling temperature
22 differently in the different control modes, using temperature
23 information obtained from the profile thermocouples and spike
24 thermocouples.

Another aspect of the invention provides a controller unit
for controlling a thermal reactor supporting a heating element,
powered by a power source, profile thermocouples and spike
thermocouples, the controller unit comprising: an on-line
model which predicts wafer temperature; and a plurality of
selectable control mode logic circuits which control the
heating element in response to the on-line model, and

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3 temperature information obtained from the profile
4 thermocouples, and spike thermocouples during operation.
5

6 Another aspect of the invention provides a method of
7 controlling a thermal reactor supporting a heating element
8 powered by a power source, profile thermocouples, and spike
9 thermocouples, the method comprising: controlling energy
10 provided to the thermal reactor relative to desired energy, by
11 using measurements from profile thermocouples and taking the
12 integral of $e^{(-2/kT)}$ where k is Boltzmann's constant and T is
13 temperature measured using the profile thermocouples.
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17 Another aspect of the invention provides a controller unit
18 for controlling a thermal reactor supporting a heating element
19 powered by a power source, profile thermocouples and spike
20 thermocouples, the controller unit comprising: a thermal
21 budget controller which controls energy provided to the thermal
22 reactor relative to desired energy, by using measurements from
23 profile thermocouples and taking the integral of $e^{(-2/kT)}$ where k
24 is Boltzmann's constant and T is temperature measured using the
profile thermocouples.

Another aspect of the invention provides a method for
controlling a thermal reactor including a thermal reactor
supporting a heating element powered by a power source, profile
thermocouples and spike thermocouples, the method comprising
the following steps: modeling thermal dynamic characteristics
of the thermal reactor; receiving a recipe including desired
temperatures with respect to time, and the recipe including
desired control modes with respect to time; and switching from

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3 one control mode to another in accordance with the recipe, and
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5 controlling temperature differently in the different control
6
7 modes, using temperature information provided by the profile
8 thermocouples and spike thermocouples, the control modes being
9 defined by cascaded controllers.

10 Another aspect of the invention provides a controller unit
11
12 for controlling a thermal reactor supporting a heating element
13
14 powered by a power source, profile thermocouples and spike
15 thermocouples, the controller unit comprising: an on-line
16
17 model which predicts wafer temperature; and a plurality of
18
19 cascaded selectable control mode logic circuits which control
20
21 the heating element in response to one or more of: the profile
22 thermocouples, spike thermocouples, and the on-line model.

23 Another aspect of the invention provides a controller unit
24
25 for controlling a thermal reactor supporting a heating element
26
27 powered by a power source, profile thermocouples and spike
28 thermocouples, the controller unit comprising an on-line model
29
30 which predicts wafer temperature based on measurements from the
31
32 spike and profile thermocouples; and a plurality of selectable
33
34 control mode logic circuits, the control mode logic circuits
35
36 including a base control mode logic circuit having a spike
37
38 controller which controls power supplied to the heating element
39
40 in response to measurements by the spike thermocouples, and a
41
42 profile controller which controls the spike controller in
43
44 response to measurements by the profile thermocouples; a
45
46 thermal budget control mode logic circuit which measures energy
47
48 provided to the thermal reactor and controls energy provided to

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3 the thermal reactor with respect to desired energy, the thermal
4 budget control mode logic circuit employing the spike
5 controller, and the profile controller, and the thermal budget
6 control mode logic circuit further including a Dt controller
7 controlling the profile controller; and a dynamic control mode
8 logic circuit which controls energy provided to the thermal
9 reactor based on predicted wafer temperature, the dynamic
10 control mode logic circuit employing the spike controller, the
11 profile controller, and the on-line model, the dynamic control
12 mode logic circuit further including a wafer controller in
13 communication with the on-line model and controlling the
14 profile controller.
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20 Fig. 1A shows a thermal reactor system 10 embodying the
21 invention. The thermal reactor system 10 includes a thermal
22 reactor 12. The thermal reactor 12 can either be horizontal or
23 vertical in orientation.
24

The thermal reactor 12 includes a process tube 14 defining
a chamber. The process tube 14 is preferably made of quartz,
or silicon carbide. In the illustrated embodiment, the process
tube is in the general shape of a hollow cylinder having an
open end 16. The process tube 14 has a length which extends
along and substantially defines a longitudinal axis. The
thermal reactor system 10 further includes a boat loader or
paddle 18 which inserts or removes a wafer load 20 into or from
the process tube 14. More particularly, the boat loader 18
includes a support portion 22, and a door portion 24 which is
movable with the support portion and which closes the open end

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3 of the process tube 14 when the support portion 22 is inserted
4 into the process tube. The door portion 24 seals and insulates
5 the process tube to prevent heat loss after the wafer load 20
6 has been inserted into the process tube 14.
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9 The wafer load 20 includes a plurality of boats 26. In
10 the illustrated embodiment, the boats 24 are formed of quartz
11 or silicon carbide. The wafer load 20 further includes a
12 plurality of silicon wafers 26, and each boat 24 supports a
13 plurality of the wafers 26. In the illustrated embodiment,
14 wafers on each boat 24 are equally spaced. The boat or boats
15 of wafers 26 generally form a wafer or other semiconductor
16 workpiece processing array.
17
18

19 The thermal reactor 12 includes a heating element 30
20 surrounding the process tube 14. In the illustrated
21 embodiment, the heating element 30 is an electrical resistance
22 heating coil or coils extending along the length of the
23 processing chamber parallel to the length of the process tube
24 14. The heating element 30 is subdivided into a plurality of
separately controllable heating zones 32. The zones 32 are
defined by providing connections along the coil to divide the
coil or coils into the separately controllable zones. The
zones are then separately controllable by supplying power to
opposite ends of each zone associated coil or portion of a
larger coil. More particularly, the thermal reactor system 10
further includes (Fig. 4) high current voltage transformers 33
and silicon controlled rectifiers (SCRs) 34 for controllably
applying power to each of the heating zones 32.

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4 The thermal reactor 12 further includes ceramic insulation
5 35 encasing the heating element 30. The insulation also serves
6 to reflect and otherwise direct heat toward the wafer array and
7 serves to provide a more uniform layer to minimize heat flux
8 variations away from the processing array.
9

10 The thermal reactor 12 further includes a plurality of
11 spike thermocouples 36. Thermocouples as the term is used
12 herein encompasses potentially a variety of temperature
13 sensors, including the more specific meaning of thermocouples.
14

15 Alternative temperature sensor constructions are intended by
16 the use of the term thermocouples. The spike thermocouples 36
17 are placed at a suitable location, such as between the heating
18 element 30 and the process tube 14. The spike thermocouples 36
19 are spaced apart along the length of the of the heating element
20 30, and a spike thermocouple 36 is located in each of the
21 heating zones 32. The spike thermocouples 36 provide the most
22 specific and responsive indications of the temperature at or of
23 the heating elements in each of the heating zones.
24

The thermal reactor 12 further includes a profile
temperature sensor sheath 38 extending inside the process tube
14. The process tube 14 has a bottom surface, and the process
tube 14 is supported on the bottom surface of the process tube
14 in an orientation parallel to the length of the process
tube. The sheath 38 extends at least partially across each of
the heating zones 32. In the illustrated embodiment, the
sheath 38 is formed of quartz or silicon carbide.

The thermal reactor 12 further includes an elongated

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3 profile rod 40 supported in the sheath 38. The profile rod 40
4 has a length parallel to the length of the process tube 14.
5 The profile rod 40 includes a plurality of thermocouples 42
6 equally spaced apart along the length of the rod 40, and one
7 thermocouple 42 is located in each of the heating zones 32.
8
9 The thermocouples 42 are not necessarily aligned with the spike
10 thermocouples 36 in the direction of the length of the process
11 tube 14. The profile rod 40 measures temperature inside the
12 process tube 14 and provides an indication of the temperature
13 of the wafer load 20 in each of the heating zones.
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17 A plurality of thermocouple instrumented wafers 44 are
18 optionally employed during modeling of the thermal reactor.
19 Fig. 1B shows the thermal reactor 12 of Fig. 1A receiving the
20 thermocouple instrumented wafers 44 during modeling. These
21 thermocouple instrumented wafers 44 are uniformly spaced across
22 the wafer load 16 to provide an accurate measurement of the
23 actual temperature of the wafers 28. The wafers or other
24 workpieces being formed of silicon or other semiconductor
materials being processed. Each of the exemplary thermocouple
instrumented wafers 44 includes a silicon wafer, and two
thermocouples 46 bonded to the silicon wafer: one on the edge
of the wafer, and one on the center of the wafer. The
thermocouples 46 of each thermocouple instrumented wafer 44 are
bonded to the silicon wafer, such as with a ceramic adhesive,
to provide accurate temperature measurements.

The thermal reactor system 10 further includes a gas
delivery system or gas panel 48 controllably injecting process

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3 gases from selectable gas supplies 50 into the process tube 14
4 to grow, diffuse, or deposit material on the surface of the
5 silicon wafers 28. The gas panel 48 includes (Fig. 3) valves
6 52 and mass flow controllers 54. The mass flow controllers 52
7 are used to measure and control flows of process gasses into
8 the process tube 14.

9
10 In some embodiments, the process tube 14 is pressurized
11 for low pressure chemical vapor deposition (LPCVD) processes.
12 In these embodiments, the thermal reactor 12 further includes
13 (Fig. 3) a pressure controller 56. In these embodiments, the
14 thermal reactor system 10 further includes a baratron or other
15 suitable pressure sensing device 58 which measures the pressure
16 in the process tube and communicates the measured pressure to
17 the pressure controller 56. Further, in these embodiments, the
18 thermal reactor system 10 further includes pumps and valves 60,
19 in communication with the pressure controller 56, to achieve
20 the desired pressure in the process tube 14.

21 In some embodiments, the thermal reactor 12 further
22 includes (Fig. 3) a torch 62 internal or external to the
23 process tube 14. The torch 62 is used for wet oxidation
24 processes by burning a ratio of hydrogen and oxygen to produce
steam in the process tube 14.

The thermal reactor system 10 includes (Fig. 2) a control
system 64 controlling the thermal reactor 12. The control
system 64 includes two subsystems: a process sequencing
subsystem 66 for process sequencing, and a temperature
subsystem 68 for temperature control. Each subsystem 64 and 66

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3 includes a microprocessor, such as an Intel PC, 286, 386, 486,
4 Pentium, or higher, or clone thereof, or Motorola 6800, 68000
5 or higher, or other microprocessor.
6

7 While other microprocessors can be used, in the
8 illustrated embodiment, the process sequencing subsystem 66
9 employs a 6800 microprocessor 70. The process sequencing
10 subsystem includes random access memory 72 and a programmable
11 EPROM 74 that stores controller logic. The process sequencing
12 subsystem 66 further includes a plurality of digital input and
13 output channels 76 as well as a plurality of analog input and
14 output channels 78. The process sequencing subsystem 66
15 further includes a plurality of serial input and output
16 channels 80 for external (remote) communication, if external
17 communication is desired. The process sequencing subsystem 66
18 follows a user defined process recipe. More particularly, the
19 thermal reactor system 10 further includes a user interface 82
20 defining an input device. While other user interfaces can be
21 employed, in the illustrated embodiment the user interface 82
22 comprises a touch screen terminal interface with which a user
23 can enter a user defined process recipe. In the process
24 recipe, the user can define, on a per step basis, step time,
gas flows, chamber pressure, temperature setpoints, and ramp
rates.

While other microprocessors can be employed, in the
illustrated embodiment, the temperature subsystem 68 includes a
486 microprocessor 84. The temperature subsystem 68 further
includes dynamic random access memory 86 for use with the

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3 microprocessor 84. For example, in the illustrated embodiment,
4 the temperature subsystem 68 controller unit includes four
5 megabytes of dynamic random access memory. The temperature
6 subsystem 68 controller unit of the illustrated embodiment
7 further includes a two megabyte flash disk 88, a dual ported
8 random access memory 90, a sixteen bit analog to digital
9 converter 92, and a PC/104 bus 94. The temperature subsystem
10 includes a plurality of multivariable controllers 96, 98, 100,
11 and 102 constructed using robust optimal control theory with
12 empirically derived models of the furnace and wafers. More
13 particularly, in the illustrated embodiment, the multivariable
14 controllers 96, 98, 100, and 102 are constructed using H-
15 Infinity control theory.
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21 In the illustrated embodiment, the control system 64
22 further includes (Fig. 3) a gas panel interface 104 connected
23 between the gas panel 48 and the process sequencing subsystem
24 68. The gas panel interface 104 provides the control system 64
with an interface to communicate with the mass flow controllers
54, the gas valves 52, the internal or external torch 62, the
pressure controller 56, the boat loader 18, etc. Further, the
gas panel interface 104 includes a plurality of hardware safety
interlocks for the thermal reactor (e.g., to ensure hydrogen
flow with a proper oxygen to hydrogen ratio, to detect a flame
from the torch 62, etc.).

In the illustrated embodiment, the control system 64
further includes (Fig. 4) a temperature interface connected
between the thermocouples 36, 42, and 44 and the temperature

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3 subsystem 68. More particularly, in the illustrated
4 embodiment, the temperature interface comprises thermocouple
5 amplifier interface boards 106. In the illustrated embodiment,
6 the temperature subsystem communicates with up to two
7 thermocouple amplifier interfaces: one for measuring spike and
8 profile thermocouples 36 and 42, and one for measuring the
9 thermocouples 46 of the thermocouple instrumented wafers 44 (if
10 thermocouple instrumented wafers are employed). In the
11 illustrated embodiment, the control system 64 further includes
12 (Fig. 4) an element firing interface 108 connected between the
13 heating element 30 and the temperature subsystem 68. The
14 element firing interface 108 includes one firing board for each
15 of the defined heating zones 32. These firing boards use a
16 zero-point switching technique to apply or discontinue power at
17 zero crossings of the voltage waveform.
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24 A process of designing the controllers 96, 98, 100, and 102 is illustrated in detail in Fig. 11.

In a characterization control mode (Fig. 6, and step 110 of Fig. 11), the thermal dynamic characteristics of the thermal reactor are modeled using spike, profile, and wafer temperatures as well as power setpoints during excitation using a random or other stimulation sequence (Fig. 5). In the illustrated embodiment, a pseudo-random binary sequence (PRBS) is employed. More particularly, in the characterization control mode (Fig. 6), the thermal reactor is brought up to operating temperature and then perturbed using the pseudo-random binary sequence, causing gradual temperature

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3 fluctuations in the thermal reactor. In steps 112a-d, models
4 are created based on changes in temperature created by the
5 perturbations. In the illustrated embodiment, all models are
6 derived using a linear least squares minimum distance system
7 identification technique. In the illustrated embodiment, all
8 models are represented and implemented in state-space form.
9
10

11 In the illustrated embodiment, two types of models are
12 created: off-line and on-line. By "off-line model," what is
13 meant is a model that is created for control system design. By
14 "on-line model," what is meant is a model that is active during
15 the operation of the thermal reactor 12, such as to process
16 actual semiconductor wafers 28.
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19 In the illustrated embodiment, three off-line models are
20 developed: a power setpoint vs. spike thermocouple model; a
21 spike thermocouple vs. profile thermocouple model; and a
22 profile and spike thermocouple vs. thermocouple instrumented
23 wafer model. Each off-line model is used to design the
24 controllers 96, 98, 100, and 102 in the temperature subsystem.

In the illustrated embodiment, a single on-line model 114
is developed to estimate wafer temperature during operation of
the thermal reactor 12. The on-line model 110 predicts the
actual temperature of the wafers 28 using real temperature
measurements from the spike and profile thermocouples 36 and
42. Because modeling of the entire thermal reactor 12 is
complicated and very susceptible to variations and maintenance
operations over time, simple modeling of the relationship
between the wafer temperatures and the measured profile and

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4 spike temperatures is performed to provide an accurate
5 indication of the wafer temperatures during dynamic changes in
6 temperature. Further, it is assumed that under steady-state
7 conditions the profile temperatures are indicative of the
8 actual temperatures of the wafers 28.
9

10 After modeling, in steps 116a, 116b, and 116c (Fig. 11),
11 the three off-line models are used to create three separate and
12 unique controllers: the spike controller 96, the profile
13 controller 98, and the wafer controller 100. The spike
14 controller 96 uses the difference between the spike setpoints
15 and spike thermocouple measurements as inputs, and then outputs
16 the power setpoints to the firing interface 108. The profile
17 controller 98 uses the difference between the profile setpoints
18 and the profile measurements as inputs and then outputs spike
19 setpoints to the spike controller 96. The wafer controller 100
20 uses the difference between the wafer setpoints and predictions
21 of the on-line wafer temperature model as inputs and then
22 outputs profile setpoints to the profile controller 98. In the
23 illustrated embodiment, each controller 96, 98, and 100 is
24 designed using H-Infinity robust optimal control theory. More
particularly, in the illustrated embodiment, each of these
controllers are multivariable, in which the interaction between
heating zones is taken into consideration to provide improved
temperature response to the desired ramp or setpoint.

The design of the controllers 96, 98, and 100 will now be
described in greater detail. The controllers 96, 98, and 100
are designed using data obtained from an identification

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3 experiment. The design procedure comprises two main steps;
4 namely, system identification and controller design. The
5 preferred embodiment employs high performance numerical
6 analysis software such as MATLAB (TM) and SIMULINK (TM) in
7 modeling and in controller design.
8
9

10 11 12 System Identification or Characterization

13 The system identification or characterization step
14 involves making empirical measurements of the processor
15 temperature response characteristics in response to known
16 thermal input. The response is measured by the spike
17 thermocouples 36, profile thermocouples 42 and the temperature
18 sensing wafers 46. The measured response data is analyzed
19 using a suitable analytical technique to achieve a model or
20 models which provide predictive indication of wafer
21 temperatures based upon the spike and profile thermocouple
22 temperatures which can be measured during actual processing of
23 wafers. However, to achieve the needed system thermal response
24 characterization it is necessary to utilize the temperature
sensing wafers 46 or other measuring techniques which at least
at this time must be done in a separate characterizing phase
before actual operational processing begins.

One preferred technique for deriving the characterization
information involves using a least-squares parameter estimation
algorithm to obtain estimates of the system parameters which
reflect temperature response characteristics. The main
objectives of this step are the identification of a system

model that describes the input-output data and the estimation of uncertainty bounds that describe the confidence in the model. For this purpose, we consider systems described by the general state-space model:

$$\dot{x} = Ax + Bu; \quad y = Cx + Du$$

where x is the state vector, u is the input vector having m number of inputs, and y is the output vector having n number of outputs. Matrix A has dimensions $n \times n$. Matrix B has dimensions $n \times m$. Matrix C has dimensions $m \times n$. And matrix D has dimensions $m \times m$. The coefficients of the matrices are parameters which are derived and potentially adjusted for the particular model being developed to optimize the model's successful operation.

Assuming that (A, C) is observable (all modes of the state-space equation can be observed at the output), the above model can be written as:

$$\dot{x} = (A - LC)x + (B - LD)u + Ly; \quad y = Cx + Du$$

where $A - LC$ is a Hurwitz matrix (see various texts on control theory, such as Kailath, T., *Linear Systems*, Prentice-Hall, Englewood Cliffs, NJ, 1980).

This implies that the above linear system can be described by:

$$\dot{x} = Fx + \Theta_1 u + \Theta_2 y; \quad y = qx + du$$

where (F, q) is observable, F is the Hurwitz matrix and Θ_1 , Θ_2 , and d are matrices representing the adjustable parameters of the model.

By taking a Laplace transform of the previous equation, we

have:

$$sIx(s) - x(0) = Fx(s) + \Theta_1 u(s) + \Theta_2 y(s); \quad y(s) = qx(s) + du(s)$$

where I is the identity matrix and $x(0)$ are the initial conditions of the states.

Next, by solving for the states we obtain:

$$x(s) = (sI - Fx)^{-1} [\Theta_1 u(s) + \Theta_2 y(s) + x(0)]$$

Now solving for the output using the above state equation to obtain:

$$y(s) = q(sI - Fx)^{-1} [\Theta_1 u(s) + \Theta_2 y(s) + x(0)] + du(s)$$

Reorganizing into common terms the above equation becomes:

$$y(s) = [q(sI - Fx)^{-1} \Theta_1 + d] u(s) + q(sI - F)^{-1} \Theta_2 y(s) + q(sI - F)^{-1} x(0)$$

All are scalar transfer functions, therefore they may be transposed to obtain:

$$y(s) = \Theta_1^T (sI - F^T)^{-1} q^T u(s) + \Theta_2^T (sI - F^T)^{-1} q^T y(s) + du(s) + x(0)^T (sI - F^T)^{-1} q^T$$

For single-input, single-output systems, the last equation can be written in the convenient for parameter estimation linear model form:

$$y = \Theta^T w$$

where Θ is a vector containing the adjustable parameters Θ_1 , Θ_2 , d as well as the possibly unknown initial conditions $x(0)$, while w contains the signals $(sI - F^T)^{-1} q^T u$, $(sI - F^T)^{-1} q^T y$, u , and $(sI - F^T)^{-1} q^T$.

Thus, the basic system identification step comprises the following sub-steps:

1. Perform an experiment to generate input-output time sequences.

2. Compute the filtered signals w .
3. Estimate the parameters of the linear model $y = \Theta^T w$.
4. Compute the corresponding state-space representation $[A, B, C, D]$ of the identified system.
5. Reduce the order of the identified system, if necessary.
6. Compute error bounds (uncertainty) for the identified system.

These substeps of the system identification step will now be described in greater detail.

The identification or characterization experiment relies on the generation of an input signal which provides sufficient excitation to the thermal reactor so as to allow the reliable identification of its parameters. Several types of excitation signals have been proposed in the literature (see, for example, Ljung, L., *System Identification: Theory for the User*, Prentice-Hall, Englewood Cliffs, NJ, 1980). For reasons of design simplicity, the illustrated embodiment employs the pseudo-random binary sequence (PRBS) to provide the desired excitation. Furthermore, in order to avoid extensive experimentation requirements in selecting the size of the excitation, the identification is performed in closed-loop. That is, prior information about the thermal reactor to be identified is used to design a simple controller (e.g., proportional or proportional-integral). The pseudo-random binary sequence excitation is then fed as a reference input (set-point) to the controller and the resulting control inputs

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3 and thermal reactor outputs are measured.
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5 Although such an approach seems restrictive in that it
6 requires a preliminary controller design, in practice this
7 requirement is not too severe. Typically, elementary crude
8 models of the thermal reactor are available or can easily be
9 derived or, as it is often the case, simple controllers have
10 been already implemented. Practical experience indicates that
11 the identification results are not too sensitive to the
12 controller used as long as its bandwidth and performance are
13 reasonable. Of course, if this is not the case, the
14 identification and controller design steps can be iterated
15 using the new controller in the next identification experiment,
16 until adequate performance is obtained.
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21 The design of the pseudo-random binary sequence requires
22 more attention. This type of excitation is implemented as a
23 sequence of step changes in the reference commands about the
24 nominal operating condition of the thermal reactor. Pseudo-
random binary sequences can be defined by two vectors:

$$[t_1, t_2, \Lambda], [m_1, m_2, \Lambda]$$

where the first vector indicates switching times and the second
indicates the deviation from the nominal set-point (\pm maximum
deviation level). The randomness in the pseudo-random binary
sequence enters in the switching times where $t_{i+1} - t_i$ is a random
number. The maximum level and the minimum and maximum duration
of each pulse are the design parameters of a pseudo-random
binary sequence. In general, the level should be selected as
large enough to provide a good signal-to-noise ratio (SNR) but

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4 small enough so as to avoid big deviations from the nominal
5 operating condition, which will introduce interference from the
6 ever-present plant nonlinearities. This is precisely where
7 closed-loop identification has an advantage because even a
8 crude controller will keep the plant response around the
9 nominal within, roughly, the PRBS level. The duration of each
10 pseudo-random binary sequence pulse should be such that the
11 resulting sequence has most of its power around the desired
12 closed-loop bandwidth (and closed-loop crossover) which is
13 where the reactor model should be reliable. Finally, the total
14 length of the pseudo-random binary sequence is dictated by
15 memory and experiment-time limitations, but it should be long
16 enough to allow for noise averaging and the observation of the
17 plant response at a sufficient number of frequencies. Roughly,
18 a rule of thumb is to observe the response of the thermal
19 reactor to 7-10 PRBS pulses whose duration is selected
20 according to the previous criteria.
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For multivariable system identification, multiple PRBS inputs must be generated, one for each channel. These should be further restricted to be independent of each other, in the sense that the resulting regressor vector has a well-conditioned covariance matrix. This requirement does not present a problem when long sequences are used. In practice, however, the limited length of the sequence suggests that the validity of this assumption should be checked and the PRBS regenerated if the condition fails.

As previously mentioned, a standard least squares

algorithm is used to estimate the parameters of the linear model which are then used to compute the entries of the state-space matrices according to the equations presented above. In addition to this, the parameter estimation algorithm is modified in order to improve its reliability and its ability to yield estimates that emphasize the fit of the plant characteristics in a given frequency range (weighted least-squares). The latter is achieved in a straightforward manner by filtering the input-output data numerically, with a filter that has a desired frequency response. For example, a low-pass filter could be used in cases of data corrupted by high-frequency noise, while a band-pass filter could be used to enhance the reliability of the identified model around the desired closed-loop bandwidth. The success of the identification and the possible redesign of these filters are judged based on "uncertainty" bounds that are discussed subsequently. It should be emphasized that although some iterations may be required in the parameter estimation step, these do not necessarily require repetition of the identification experiment.

Further, and in order to improve the numerical reliability of the estimator, singular value decomposition methods are employed to compute the least-squares solution. In addition to this, the estimation step solves, in one embodiment, the following problem

$$\text{Min } \|H\Theta\|, \text{ subject to: } \|y - \Theta w\| \leq (1+\rho) E_{LS}$$

where H is a weighting matrix, ρ is a threshold parameter and

E_{LS} is the error corresponding to the least-squares solution. While this problem can be solved easily in closed form, its solution possesses some interesting properties. That is, by choosing the threshold parameter to be sufficiently "small" (e.g., 0.5) the quality of the estimated parameters measured by the estimation error deteriorates in a controlled fashion, by at most a factor of $(1+\rho)$. This allows the flexibility to adjust the estimated parameters so as to reflect more subtle estimation objectives. For example, by appropriately choosing the weighting matrix H , the solution of the above minimization can emphasize coupling and/or stability properties of the identified model. This ability has been found to be beneficial in cases of noisy data where the noise may cause the reactor to appear as more coupled than it is in "reality." Alternatively, it may be desirable for a reactor model to be as decoupled as possible, something that simplifies the controller design and can possibly improve its robustness to reactor variations.

The obtained reactor model is then checked for minimality using standard reduction algorithms, (see Chiang, R. and M. Safonov, *Robust Control Toolbox: User's Manual (For use with MATLAB)*, The Mathworks Inc., Natick, MA, 1992) and references therein, and the reliability of the model is quantified by analysis of residuals. This step quantifies confidence in the model and provides constraints that should be met during the controller design step. In particular, performing a spectral analysis on the estimation error provides estimates of the effective multiplicative and feedback uncertainty (see

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3 Alexander, C. and K.S. Tsakalis, "Control of an Inverted
4 Pendulum: A Classical Experiment Revisited," *Proc. 1995 Western*
5 *Multiconference, Society for Computer Simulation, Las Vegas,*
6 *1995).* These estimates represent bounds that the closed-loop
7 sensitivity and complementary sensitivity should satisfy so
8 that the designed controller will stabilize the actual reactor.
9

10 It should be pointed out that the computations provide only an
11 estimate of these bounds. In a strict sense, closed-loop
12 stability cannot be guaranteed. However, there appears to be a
13 very strong correlation between these bounds and successful
14 controller designs.
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Controller Design

The core of the controller design procedure is the H^∞ design approach (see Chiang, R. and M. Safonov, *Robust Control Toolbox: User's Manual (For use with MATLAB)*, The Mathworks Inc., Natick, MA, 1992), augmented by controller reduction and well-posedness checks. More specifically, the uncertainty bounds resulting from the system identification step are used to define sensitivity and complementary sensitivity weights. These, together with the identified reactor, augmented by integrators, form the so-called super-plant in the format required by standard H^∞ computational software. Typically, the resulting H^∞ controller is of high order and contains states due to the weights that are essentially irrelevant for its performance and can potentially degrade its reliability, robustness and discretization properties. For this reason, the reduction is performed in three steps.

The first step is to remove states that correspond to very fast modes, e.g., two orders of magnitude above the closed-loop bandwidth. Typically, such modes are irrelevant to the controller stability or performance but they create problems in digital implementation since their discrete-time approximation requires high sampling rates. The next step is to remove very slow modes which again contribute very little to the overall closed-loop behavior. Such modes are typically associated with "pole-zero cancellations" near the $j\omega$ -axis and, if retained, may cause the appearance of small but slowly decaying errors in the tracking performance. Finally, a standard model order

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4 reduction (weighted or not) is performed to eliminate other
5 controller states that have insignificant contribution. The
6 reduction step is a price paid in order to simplify the weight
7 selection step. Even though a verification is made that the
8 reductions did not cause any significant performance
9 deterioration, this verification is relatively straightforward
10 and can be performed easily with standard computational tools,
11 e.g., (see Chiang, R. and M. Safonov, *Robust Control Toolbox:
12 User's Manual (For use with MATLAB)*, The Mathworks Inc.,
13 Natick, MA, 1992, and Zhou, K., J. Doyle and K. Glover, *Robust
14 and Optimal Control*, Prentice-Hall, Englewood Cliffs, NJ,
15 1996).

16
17 The above procedure computes a controller of reasonable
18 order that exhibits good performance with the linearized model
19 of the reactor. That is, the actual system is expected to
20 exhibit similar performance locally around the operating point.

21 For a successful controller implementation, however,
22 saturation nonlinearities that are invariably present in all
23 actuators, e.g., heating elements, should be considered. The
24 main problem caused by such saturations is the so-called
integrator wind-up. Typical anti-windup modifications include
the use of a stabilizing feedback around the compensator that
is activated by a dead-zone type nonlinearity when the
controller output (control input) exceeds the saturation level
(see Astrom, K.J. and B. Hagglund, *PID Controllers: Theory,
Design and Tuning*, ISA Research Triangle Park, NC, 1994).

A simple way to achieve this in the multivariable case, is

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3 by feeding back to the compensator an auxiliary signal "v"
4 computed as
5

$$v = Lud(u)$$

6
7 where u is the control input, d(u) is a scalar, dead-zone-like
8 signal quantifying the level of saturation (d(u)=0 when the
9 control is not saturated) and L is a matrix gain such that the
10 closed-loop system of the controller and L is stable. An
11 effective design of L can be obtained as an observer gain (see
12 Anderson, B.D.O. and J.B. Moore, *Optimal Control: Linear*
13 *Quadratic Methods*, Prentice-Hall, Englewood Cliffs, NJ, 1990).
14
15

16 In this case, the controller-observer gain system can be
17 nicely interpreted as the construction of an observer which
18 forces the controller output to track the output of a system
19 that consists of the controller composed with the saturation
20 nonlinearity. This, together with the minimality of the
21 controller ensure that its states, and in particular those
22 associated with the integrators cannot grow unbounded.
23 Furthermore, in the design of the observer gain, the
24 directionality properties of the controller can be preserved as
much as possible, so that the controller saturation does not
completely destroy the output decoupling achieved by the linear
design.

Finally, as a last step in the controller design
procedure, an evaluation step is performed via nonlinear
simulation of the discretized controller and identified
reactor, together with the actuator saturation. This
evaluation has been very useful in exposing possible design

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3 limitations and assessing the controller capabilities, e.g., in
4 terms of achievable ramp rates. Practical experience indicates
5 that the simulated behavior of the closed loop system is indeed
6 a good approximation of the actual one.
7
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9 After design, in step 118, the spike, profile, and wafer
10 controllers 96, 98, and 100 and the on-line wafer model are
11 implemented in hardware in the temperature subsystem 68.
12

13 In the illustrated embodiment, a control mode logic
14 circuit is selectable from among different available control
15 mode logic circuits including an element control mode logic
16 circuit (Fig. 7) defining an element control mode, a base
17 control mode logic circuit (Fig. 8) defining a base control
18 mode, a dynamic control mode logic circuit (Fig. 9) defining a
19 dynamic control mode, and a Dt control mode logic circuit (Fig.
20 10) defining a Dt control mode. Each of these control mode
21 logic circuits are defined by a single one or a combination of
22 the controllers 96, 98, and 100.
23
24

More particularly, the temperature subsystem 68 employs
the spike controller 96 for the element control mode (Fig. 7).

The temperature subsystem 68 employs the spike controller 96
injected with the pseudo-random binary sequence for the
characterization control mode (Fig. 6). The temperature
subsystem 68 employs a combination of the profile controller 98
and the spike controller 96 for the base control mode (Fig. 8).

The temperature subsystem 68 employs a combination of the
wafer controller 100, the profile controller 98, and the spike
controller 96 for the dynamic control mode (Fig. 9). The

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3 temperature subsystem 68 employs the non-linear Dt controller
4 102 with the profile controller 98, and the spike controller 96
5 to provide the Dt control mode (Fig. 10).
6

7
8 A user can provide a recipe comprising multiple steps and
9 which uses any one of the control modes in each step. For
10 example, a user can provide a recipe that switches from one
11 control mode to another at a given stage of semiconductor
12 processing. One suggested approach is to employ the base
13 control mode during a furnace check and push in of the boat 18,
14 prior to a ramp up in temperature, to employ the wafer control
15 mode during temperature ramp up and temperature stabilization,
16 to employ the Dt control mode during wafer processing steps,
17 and to employ the base control mode during boat push out.
18 Another suggested approach is to use the base control mode
19 during all processing steps.
20
21

22 The element control mode is typically a maintenance mode
23 (e.g., to burn in elements). In the element control mode, the
24 spike controller controls on the basis of spike thermocouple
temperatures. The mode is not used in normal processing of
wafers.

The base control mode (Fig. 8) is the default mode of
operation. In the base control mode, the profile controller 98
provides a spike setpoint control signal based on a profile
error. The profile error is based on the difference between
profile temperature setpoint, and profile temperature
measurements by the profile thermocouples 42. The spike
controller 98 controls power to the thermal reactor based on

1 spike error. The spike error is based on the difference
2
3 between spike setpoint and spike temperature measurements by
4
5 the spike thermocouples 36. The base control mode provides
6
7 accurate control resulting in improved process uniformity and
8
9 cycle time reduction attributed to faster stabilization times.

10 The base control mode logic circuit uses the profile and spike
11
12 controllers simultaneously by cascading them together.

13 Profile thermocouples do not match temperatures at the
14
15 edge of a load. Users prefer not to change their recipes to
16
17 compensate for this. One solution to this problem is to
18
19 shorten profile thermocouples which results in readings
20
21 generated by the profile thermocouples more accurately matching
22
23 temperatures at the edge of a load. The dynamic or wafer
24
control mode (Fig. 9) provides a solution to the problem
without requiring modification of the profile thermocouples or
adjustment of the user's recipe.

In the dynamic control mode, the wafer controller 100
provides prediction or estimation of the temperatures of wafers
28 and control to achieve temperatures for the wafers 28 which
approach the desired or recipe wafer temperatures. The dynamic
control mode may be most advantageously employed during
temperature ramping and stabilization steps. The dynamic
control mode involves the prior use of the thermocouple
instrumented wafers 44 during modeling, as discussed above.
After modeling, while the control system is in use, the dynamic
control mode controls the thermal reactor 12 based on predicted
wafer temperature using the on-line wafer temperature

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4 estimating model 114. The on-line wafer temperature estimation
5 model 114 predicts wafer temperature based on measurements from
6 the spike and profile thermocouples 36 and 42. More
7 particularly, wafer temperature is predicted based on
8 measurements from the spike and profile thermocouples 36 and 42
9 and the relationship between measurements taken by the
10 thermocouple instrumented wafers 44 (representing wafer
11 temperature) and measurements taken by the profile and spike
12 thermocouples 36 and 42 during modeling.

13
14
15 In the dynamic control mode, the wafer controller 100
16 provides a profile setpoint based on a wafer error. The wafer
17 error is based on the difference between profile temperature
18 setpoint, and profile temperature measurements by the profile
19 thermocouples 42. The profile controller provides a spike
20 setpoint control signal based on profile error. The profile
21 error is based on the difference between profile temperature
22 setpoint produced by the wafer controller 100, and profile
23 temperature measurements by the profile thermocouples. The
24 spike controller controls power to the thermal reactor based on
spike error. The spike error is based on the difference
between spike setpoint and spike temperature measurements by
the spike thermocouples 36. The dynamic control mode uses the
spike controller 96, the profile controller 98, and the wafer
controller 100 cascaded together.

In the Dt or thermal budget mode, the Dt controller 102
measures temperature exposure or applied thermal energy and
controls energy with respect to setpoint or desired energy.

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3 Thermal budget is controlled, using measurements from profile
4 thermocouples 42 and taking the integral of $e^{(-2/kT)}$ where k is
5 Boltzmann's constant and T is temperature measured using the
6 profile thermocouples 42, to maintain Dt values in accordance
7 with desired energy. A calculation is made of energy sent into
8 the thermal reactor, and energy sent into the thermal reactor
9 is controlled. The thermal budget mode is advantageously used
10 to control thermal budget during critical processing steps to
11 maintain consistent Dt values both down the load and
12 run-to-run.
13
14
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16

17 In the Dt control mode (Fig. 10), the Dt controller 102
18 provides a profile setpoint based on an energy error. The
19 energy error is based on the difference between an energy
20 setpoint, and measured energy. The profile controller 98
21 provides a spike setpoint control signal based on a profile
22 error. The profile error is based on the difference between
23 profile temperature setpoint produced by the Dt controller, and
24 profile temperature measurements by the profile thermocouples
42. The spike controller 96 controls power to the thermal
reactor based on spike error. The spike error is based on the
difference between spike setpoint and spike temperature
measurement by the spike thermocouples 36.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred

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3 forms of putting the invention into effect. The invention is,
4 therefore, claimed in any of its forms or modifications within
5 the proper scope of the appended claims appropriately
6 interpreted in accordance with the doctrine of equivalents.
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CLAIMS:

1. A method for controlling a thermal reactor including a heating element powered by a power source, and having profile thermocouples and spike thermocouples, the method comprising the following steps:

modeling thermal dynamic characteristics of the thermal reactor, the modeling step including providing thermocouple instrumented wafers in the thermal reactor, perturbing the thermal reactor by controlling the heating element using a stimulation sequence, and developing models based on changes in temperature created by the perturbations, the models including a model of power versus spike thermocouple readings, a model of spike thermocouple readings versus profile thermocouple readings, and a model of profile and spike thermocouple readings versus thermocouple instrumented wafer readings.

2. A method for controlling a thermal reactor in accordance with claim 0 and further comprising, after the modeling step, selecting a control mode from among a plurality of available control modes.

3. A method for controlling a thermal reactor in accordance with claim 0 wherein one of the available control modes is a thermal budget control mode in which energy provided to the thermal reactor is measured and controlled with respect to desired energy.

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3 4. A method for controlling a thermal reactor in
4 accordance with claim 0 wherein one of the available control
5 modes is a thermal budget control mode wherein energy provided
6 to the thermal reactor is controlled relative to desired
7 energy, by using measurements from profile thermocouples and
8 taking the integral of $e^{(-2/kT)}$ where k is Boltzmann's constant
9 and T is temperature measured using the profile thermocouples.
10
11
12

13
14 5. A method for controlling a thermal reactor in
15 accordance with claim 0 wherein one of the available control
16 modes is a dynamic control mode in which power is controllably
17 supplied to the heating element based on predicted wafer
18 temperature, and in which wafer temperature is predicted based
19 on measurements from the spike and profile thermocouples.
20
21
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23 6. A method for controlling a thermal reactor in
24 accordance with claim 0 wherein one of the available control
modes is a base control mode, in which power is controllably
supplied to the heating element in response to profile
thermocouple measurements.

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3 7. A controller unit for controlling a thermal reactor
4 including a heating element powered by a power source, and
5 having profile thermocouples and spike thermocouples, and
6 selectively receiving thermocouple instrumented wafers, the
7 controller unit comprising:
8

9 an input device receiving a recipe; and
10

11 a plurality of selectable control mode logic circuits
12 communicating with the profile thermocouples and spike
13 thermocouples, the control mode logic circuits being used to
14 control the heating element relative to the recipe.
15
16
17

18 8. A controller unit in accordance with claim 0 wherein
19 the control mode logic circuits comprise H₂ controllers.
20
21

22 9. A controller unit in accordance with claim **Error!**
23 **Reference source not found.** wherein the control mode logic
24 circuits include a thermal budget control mode logic circuit
which measures energy provided to the thermal reactor and
controls energy provided to the thermal reactor with respect to
desired energy.

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3 10. A controller unit in accordance with claim **Error!**
4 **Reference source not found.** wherein the control mode logic
5 circuits include a thermal budget control mode logic circuit
6 which controls energy provided to the thermal reactor relative
7 to desired energy, by using measurements from profile
8 thermocouples and taking the integral of $e^{(-2/kT)}$ where k is
9 Boltzmann's constant and T is temperature measured using the
10 profile thermocouples.
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15 11. A controller unit in accordance with claim **Error!**
16 **Reference source not found.** wherein the control mode logic
17 circuits include a dynamic control mode logic circuit which
18 controllably supplies power to the heating element based on
19 predicted wafer temperature, the dynamic control mode logic
20 circuit including an on-line wafer model in which wafer
21 temperature is predicted based on measurements from the spike
22 and profile thermocouples.
23
24

12. A controller unit in accordance with claim **Error!**
Reference source not found. wherein the control mode logic
circuits include a base control mode logic circuit which
controls power supplied to the heating element in response to
measurements by the profile thermocouples.

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3 13. A method for controlling a thermal reactor including
4 a heating element powered by a power source, and having profile
5 thermocouples, spike thermocouples, and selectively receiving
6 thermocouple instrumented wafers, the method comprising the
7 following steps:
8

9
10 modeling thermal dynamic characteristics of the thermal
11 reactor using the profile thermocouples, spike thermocouples,
12 and instrumented wafers;
13

14 receiving a recipe including desired temperatures with
15 respect to time, and the recipe including desired control modes
16 with respect to time; and
17

18 switching from one control mode to another in accordance
19 with the recipe, and controlling temperature differently in the
20 different control modes, using the profile thermocouples and
21 spike thermocouples.
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14. A method for controlling a thermal reactor in
accordance with claim 0 wherein one of the available control
modes is a thermal budget mode wherein energy provided to the
thermal reactor is measured and controlled with respect to
desired energy.

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3 15. A method for controlling a thermal reactor in
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5 accordance with claim 0 wherein one of the available control
6
7 modes is a thermal budget mode wherein energy provided to the
8
9 thermal reactor is controlled relative to desired energy, by
10
11 using measurements from profile thermocouples and taking the
12
13 integral of $e^{(-2/kT)}$ where k is Boltzmann's constant and T is
14
15 temperature measured using the profile thermocouples.
16

17 16. A method for controlling a thermal reactor in
18
19 accordance with claim 0 wherein one of the available control
20
21 modes is a dynamic control mode in which power is controllably
22
23 supplied to the heating element based on predicted wafer
24
25 temperature, and in which wafer temperature is predicted based
26
27 on measurements from the spike and profile thermocouples.
28

29 17. A method for controlling a thermal reactor in
30
31 accordance with claim 0 wherein one of the available control
32
33 modes is a base control mode, wherein a base controller acts in
34
35 response to profile thermocouple measurements.
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3 18. A controller unit for controlling a thermal reactor
4 including a heating element powered by a power source, and
5 having profile thermocouples and spike thermocouples, the
6 controller unit comprising:
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8 an on-line model which predicts wafer temperature; and
9

10 a plurality of selectable control mode logic circuits
11 which control the heating element in response to the on-line
12 model, the profile thermocouples, and spike thermocouples.
13
14

15 19. A controller unit in accordance with claim 0 wherein
16 the control mode logic circuits include a thermal budget
17 control mode logic circuit which measures energy provided to
18 the thermal reactor and controls energy provided to the thermal
19 reactor with respect to desired energy.
20
21

22 20. A controller unit in accordance with claim 0 wherein
23 the control mode logic circuits include a thermal budget
24 control mode logic circuit, which controls energy provided to
the thermal reactor relative to desired energy, by using
measurements from profile thermocouples and taking the integral
of $e^{(-2/kT)}$ where k is Boltzmann's constant and T is temperature
measured using the profile thermocouples.

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3 21. A controller unit in accordance with claim 0 wherein
4 the control mode logic circuits include a dynamic control mode
5 logic circuit which controllably supplies power to the heating
6 element based on predicted wafer temperature, the dynamic
7 control mode logic circuit including an on-line wafer model in
8 which wafer temperature is predicted based on measurements from
9 the spike and profile thermocouples.
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14 22. A controller unit in accordance with claim 0 wherein
15 the control mode logic circuits include a base control mode
16 logic circuit which controls power supplied to the heating
17 element in response to measurements by the profile
18 thermocouples.
19
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21
22 23. A method of controlling a thermal reactor including a
23 heating element powered by a power source, and having profile
24 thermocouples and spike thermocouples, the method comprising:

controlling energy provided to the thermal reactor
relative to desired energy, by using measurements from profile
thermocouples and taking the integral of $e^{(-2/kT)}$ where k is
Boltzmann's constant and T is temperature measured using the
profile thermocouples.

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3 24. A controller unit for controlling a thermal reactor
4 including a heating element powered by a power source, and
5 having profile thermocouples and spike thermocouples, the
6 controller unit comprising:
7

8 a thermal budget controller which controls energy provided
9 to the thermal reactor relative to desired energy, by using
10 measurements from profile thermocouples and taking the integral
11 of $e^{(-2/kT)}$ where k is Boltzmann's constant and T is temperature
12 measured using the profile thermocouples.
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17 25. A method for controlling a thermal reactor including
18 a thermal reactor including a heating element powered by a
19 power source, and having profile thermocouples and spike
20 thermocouples, the method comprising the following steps:
21

22 modeling thermal dynamic characteristics of the thermal
23 reactor;
24

receiving a recipe including desired temperatures with
respect to time, and the recipe including desired control modes
with respect to time; and

switching from one control mode to another in accordance
with the recipe, and controlling temperature differently in the
different control modes, using the profile thermocouples and
spike thermocouples, the control modes being defined by
cascaded controllers.

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3 26. A method for controlling a thermal reactor in
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5 accordance with claim 0 wherein the temperature in the thermal
6 reactor is selectively ramped up to operating temperature, and
7 wherein the control modes provide full time cascade control,
8 including cascade control after the temperature is ramped up.
9
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11 27. A method for controlling a thermal reactor in
12
13 accordance with claim 0 wherein one of the available control
14 modes is a base control mode in which a spike controller acts
15 in response to spike thermocouple measurements, and in which a
16 profile controller acts in response to profile thermocouple
17 measurements and controls the spike controller.
18
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21 28. A method for controlling a thermal reactor in
22
23 accordance with claim 0 wherein one of the available control
24 modes is a thermal budget mode in which a spike controller acts
in response to spike thermocouple measurements, in which a
profile controller acts in response to profile thermocouple
measurements and controls the spike controller, and in which a
Dt controller measures energy provided to the thermal reactor
and controls energy provided to the thermal reactor with
respect to desired energy and controls the profile controller.

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3 29. A method for controlling a thermal reactor in
4 accordance with claim 0 wherein one of the available control
5 modes is a thermal budget mode in which a spike controller acts
6 in response to spike thermocouple measurements, in which a
7 profile controller acts in response to profile thermocouple
8 measurements and controls the spike controller, and in which a
9 Dt controller controls energy provided to the thermal reactor
10 relative to desired energy, by using measurements from profile
11 thermocouples and taking the integral of $e^{(-2/KT)}$ where k is
12 Boltzmann's constant and T is temperature measured using the
13 profile thermocouples, the Dt controller controlling the
14 profile controller.
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21 30. A method for controlling a thermal reactor in
22 accordance with claim 0 wherein one of the available control
23 modes is a dynamic control mode in which a spike controller
24 acts in response to spike thermocouple measurements, in which a
profile controller acts in response to profile thermocouple
measurements and controls the spike controller, and in which a
wafer controller acts in response to predicted wafer
temperature using an on-line wafer temperature estimation model
to predict the wafer temperature, the wafer controller
controlling the profile controller.

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3 31. A controller unit for controlling a thermal reactor
4 supporting a heating element powered by a power source, profile
5 thermocouples and spike thermocouples, the controller unit
6 comprising:
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8 an on-line model which predicts wafer temperature; and
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10 a plurality of cascaded selectable control mode logic
11 circuits which control the heating element in response to one
12 or more of: the profile thermocouples, spike thermocouples,
13 and the on-line model.
14

15
16 }
17 32. A controller unit in accordance with claim 0 wherein
18 the control mode logic circuits include a base control mode
19 logic circuit including a spike controller which controls power
20 supplied to the heating element in response to measurements by
21 the spike thermocouples, and a profile controller which
22 controls the spike controller in response to measurements by
23 the profile thermocouples.
24

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3 33. A controller unit in accordance with claim 0 wherein
4 the control mode logic circuits include a thermal budget
5 control mode logic circuit which measures energy provided to
6 the thermal reactor and controls energy provided to the thermal
7 reactor with respect to desired energy, the thermal budget
8 control mode logic circuit including a spike controller which
9 controls power supplied to the heating element in response to
10 measurements by the spike thermocouples, a profile controller
11 which controls the spike controller in response to measurements
12 by the profile thermocouples, and a Dt controller controlling
13 the profile controller.
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20 34. A controller unit in accordance with claim 0 wherein
21 the control mode logic circuits include a thermal budget
22 control mode logic circuit which measures energy provided to
23 the thermal reactor and controls energy provided to the thermal
24 reactor with respect to desired energy, the thermal budget
control mode logic circuit including a spike controller which
controls power supplied to the heating element in response to
measurements by the spike thermocouples, a profile controller
which controls the spike controller in response to measurements
by the profile thermocouples, and a non-linear controller
controlling the profile controller.

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3 35. A controller unit in accordance with claim 0 wherein
4 the control mode logic circuits include a thermal budget
5 control mode logic circuit which measures energy provided to
6 the thermal reactor and controls energy provided to the thermal
7 reactor with respect to desired energy, by using measurements
8 from the profile thermocouples and taking the integral of $e^{(-2/kT)}$
9 where k is Boltzmann's constant and T is temperature measured
10 using the profile thermocouples, the thermal budget control
11 mode logic circuit including a spike controller which controls
12 power supplied to the heating element in response to
13 measurements by the spike thermocouples, a profile controller
14 which controls the spike controller in response to measurements
15 by the profile thermocouples, and a Dt controller controlling
16 the profile controller.
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36. A controller unit in accordance with claim 0 wherein
the control mode logic circuits include a dynamic control mode
logic circuit which controllably supplies power to the heating
element based on predicted wafer temperature, and includes an
on-line wafer temperature model in which wafer temperature is
predicted based on measurements from the spike and profile
thermocouples.

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3 37. A controller unit in accordance with claim 0 wherein
4 the control mode logic circuits include a dynamic control mode
5 logic circuit which controllably supplies power to the heating
6 element based on predicted wafer temperature, and includes an
7 on-line wafer temperature model in which wafer temperature is
8 predicted based on measurements from the spike and profile
9 thermocouples, the dynamic control mode logic circuit including
10 a spike controller which controls power supplied to the heating
11 element in response to measurements by the spike thermocouples,
12 a profile controller which controls the spike controller in
13 response to measurements by the profile thermocouples, and a
14 wafer controller controlling the profile controller in response
15 to the on-line wafer temperature model.
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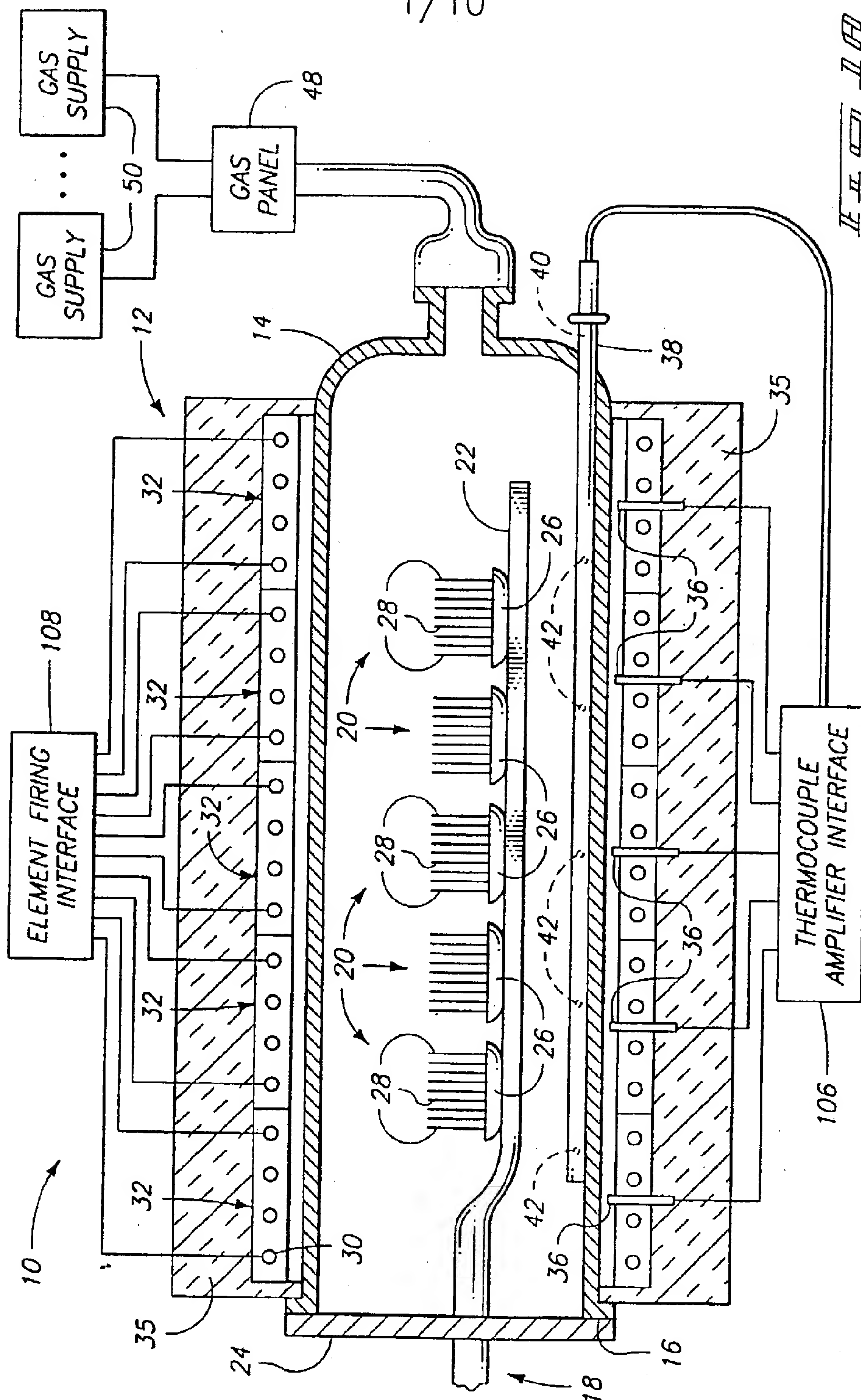
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3 38. A controller unit for controlling a thermal reactor
4 including a heating element powered by a power source, and
5 having profile thermocouples and spike thermocouples, the
6 controller unit comprising:
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9 an on-line model which predicts wafer temperature based on
10 measurements from the spike and profile thermocouples; and
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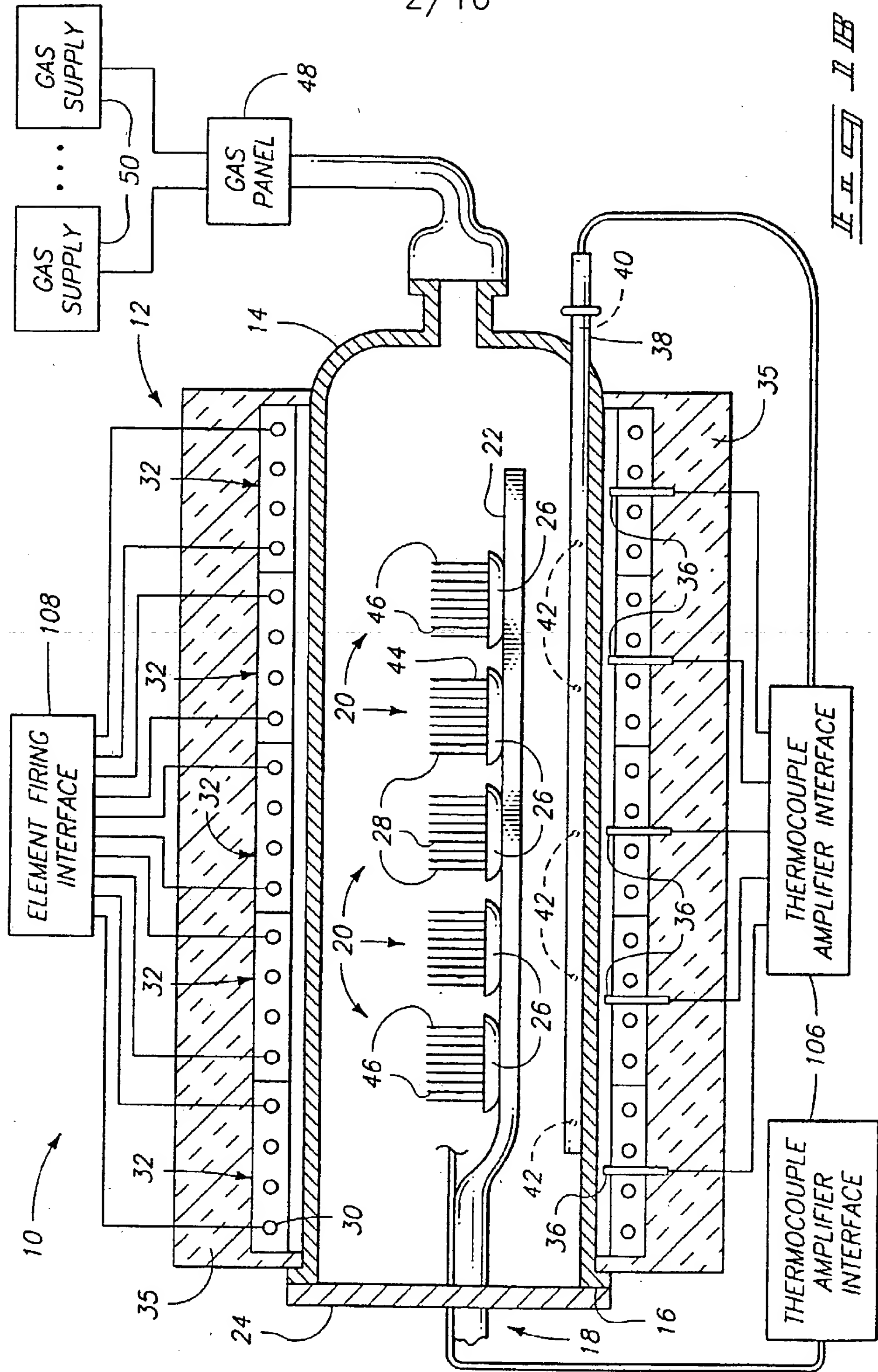
12 a plurality of selectable control mode logic circuits, the
13 control mode logic circuits including a base control mode logic
14 circuit having a spike controller which controls power supplied
15 to the heating element in response to measurements by the spike
16 thermocouples, and a profile controller which controls the
17 spike controller in response to measurements by the profile
18 thermocouples; a thermal budget control mode logic circuit
19 which measures energy provided to the thermal reactor and
20 controls energy provided to the thermal reactor with respect to
21 desired energy, the thermal budget control mode logic circuit
22 employing the spike controller, and the profile controller, and
23 the thermal budget control mode logic circuit further including
24 a Dt controller controlling the profile controller; and a
dynamic control mode logic circuit which controls energy
provided to the thermal reactor based on predicted wafer
temperature, the dynamic control mode logic circuit employing
the spike controller, the profile controller, and the on-line
model, the dynamic control mode logic circuit further including
a wafer controller in communication with the on-line model and
controlling the profile controller.

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3 39. A controller unit in accordance with claim 0 wherein
4 the controllers are respectively derived from off-line models.
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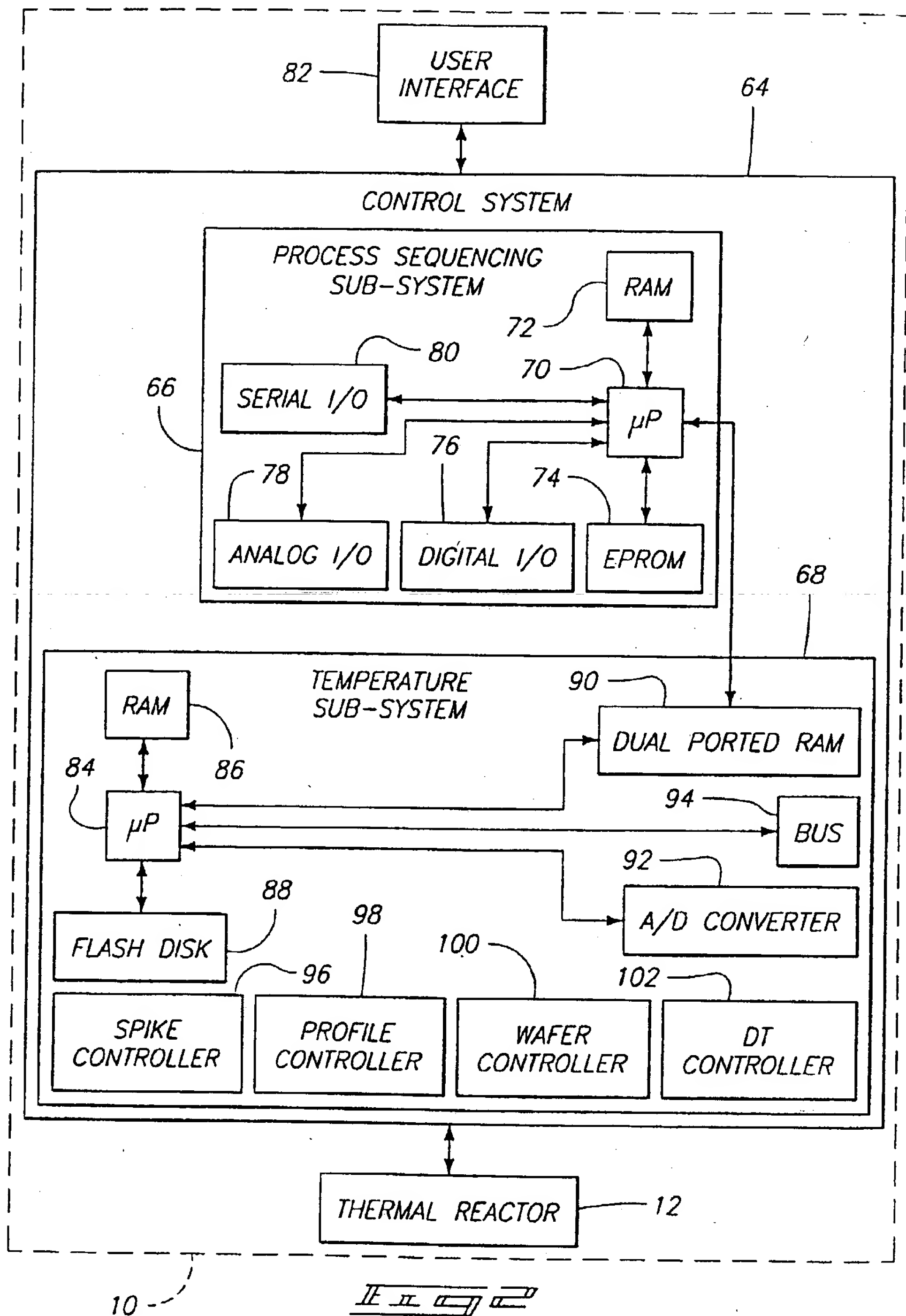
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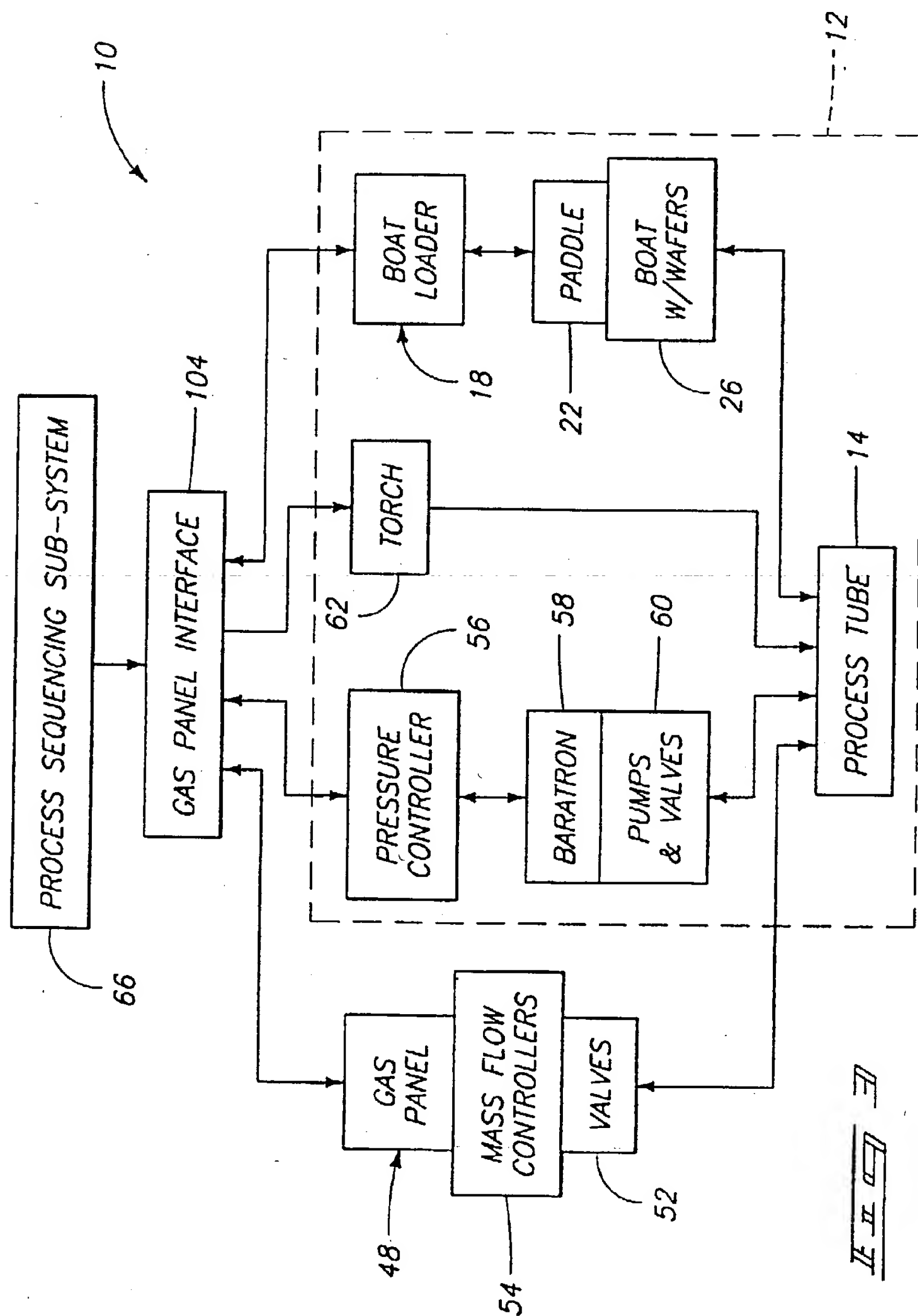
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FIG. 2

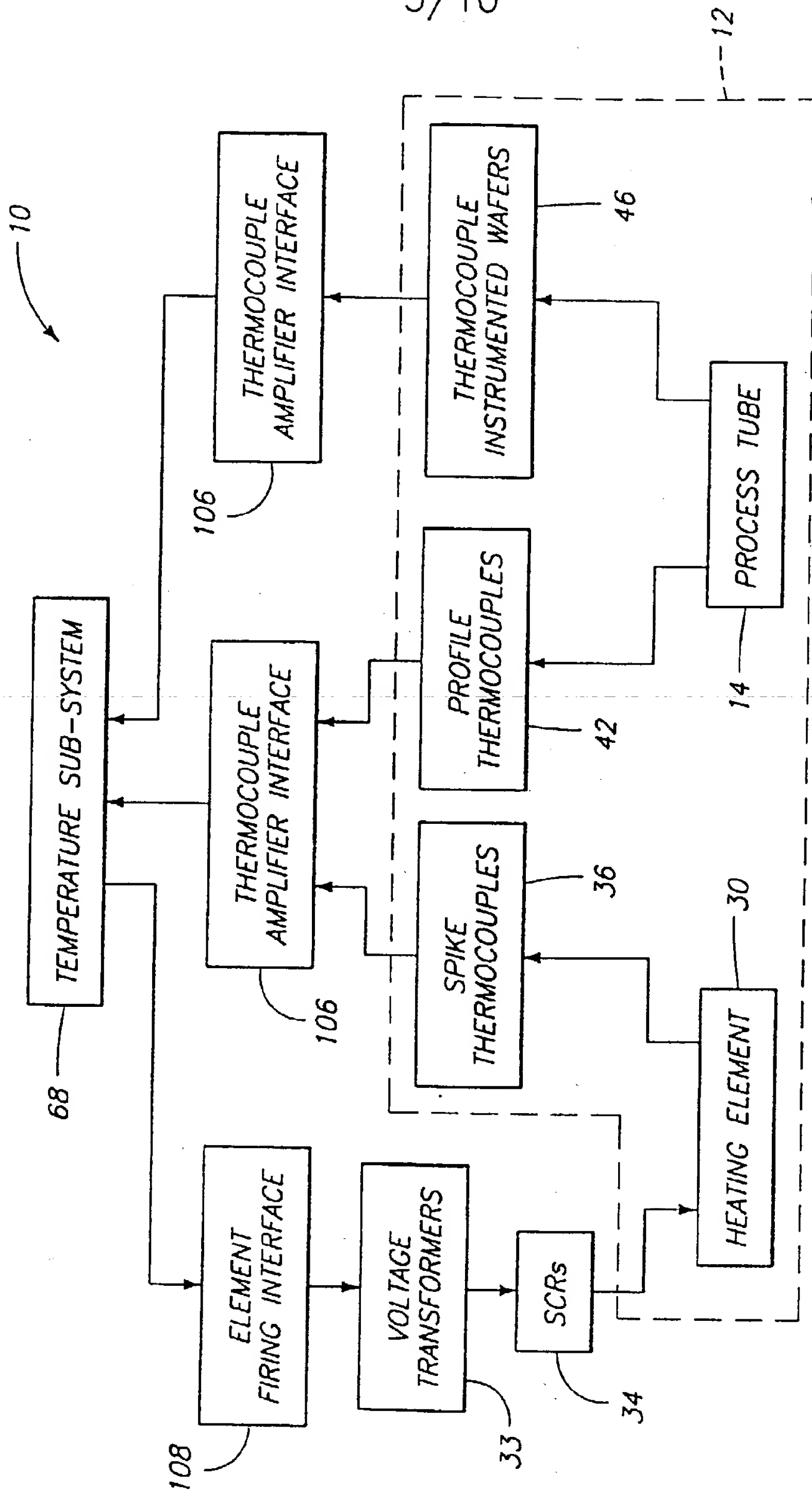
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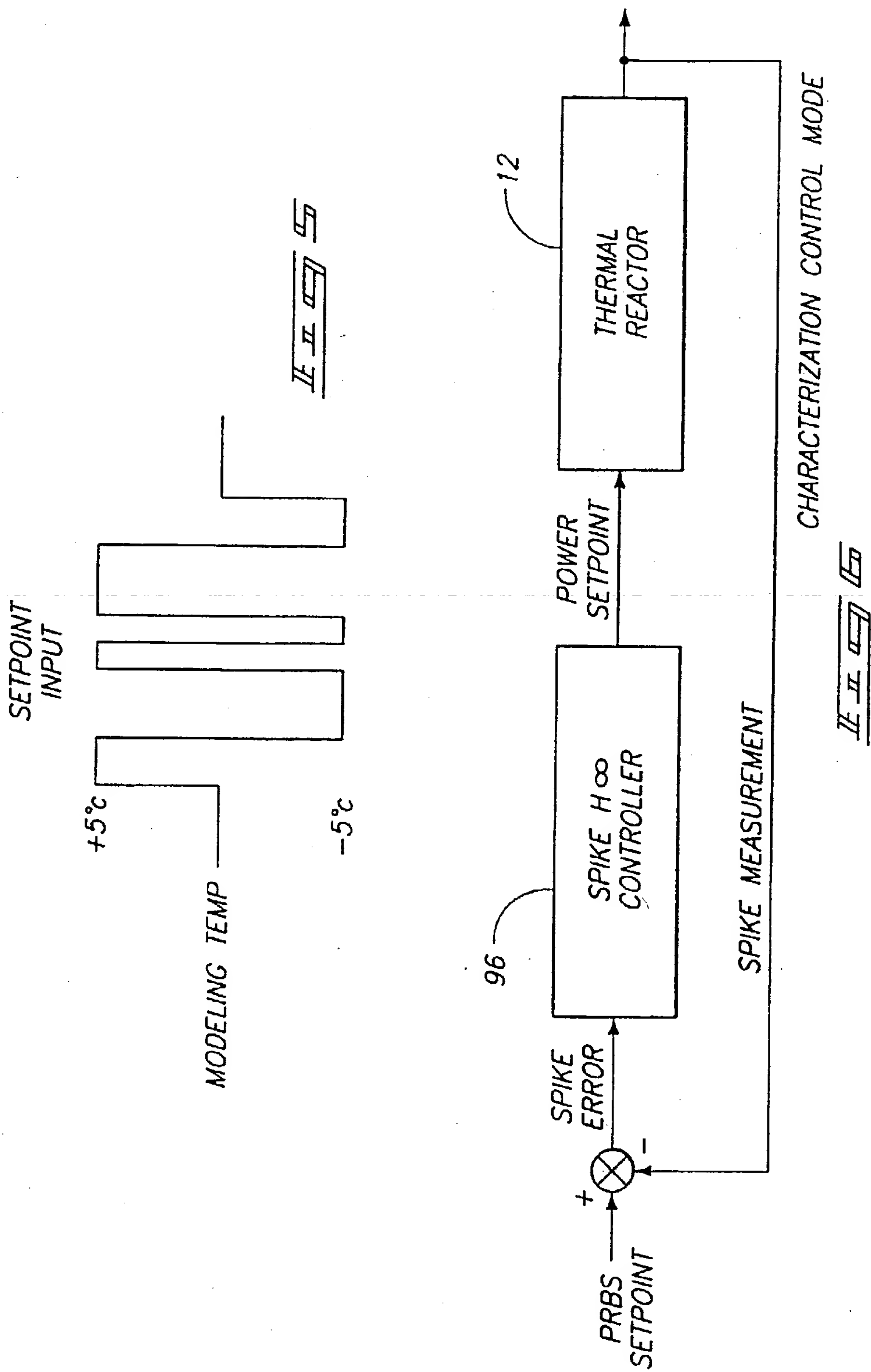
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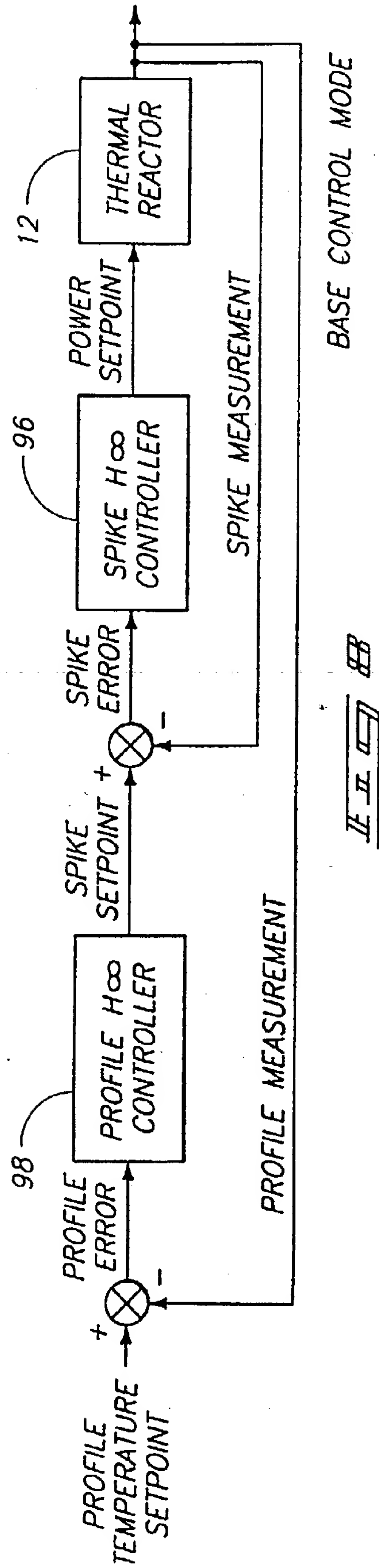
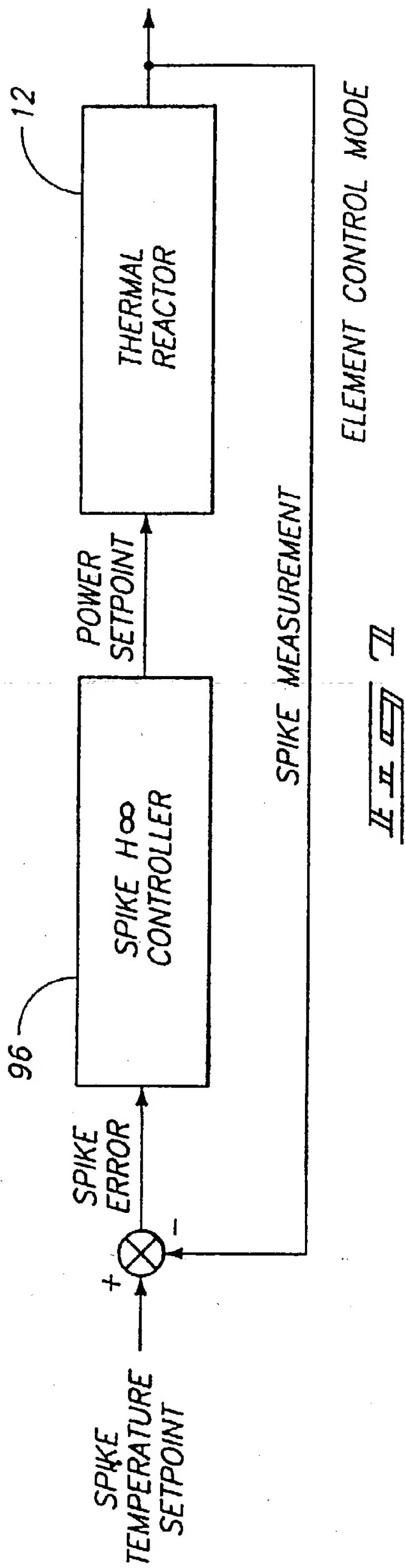
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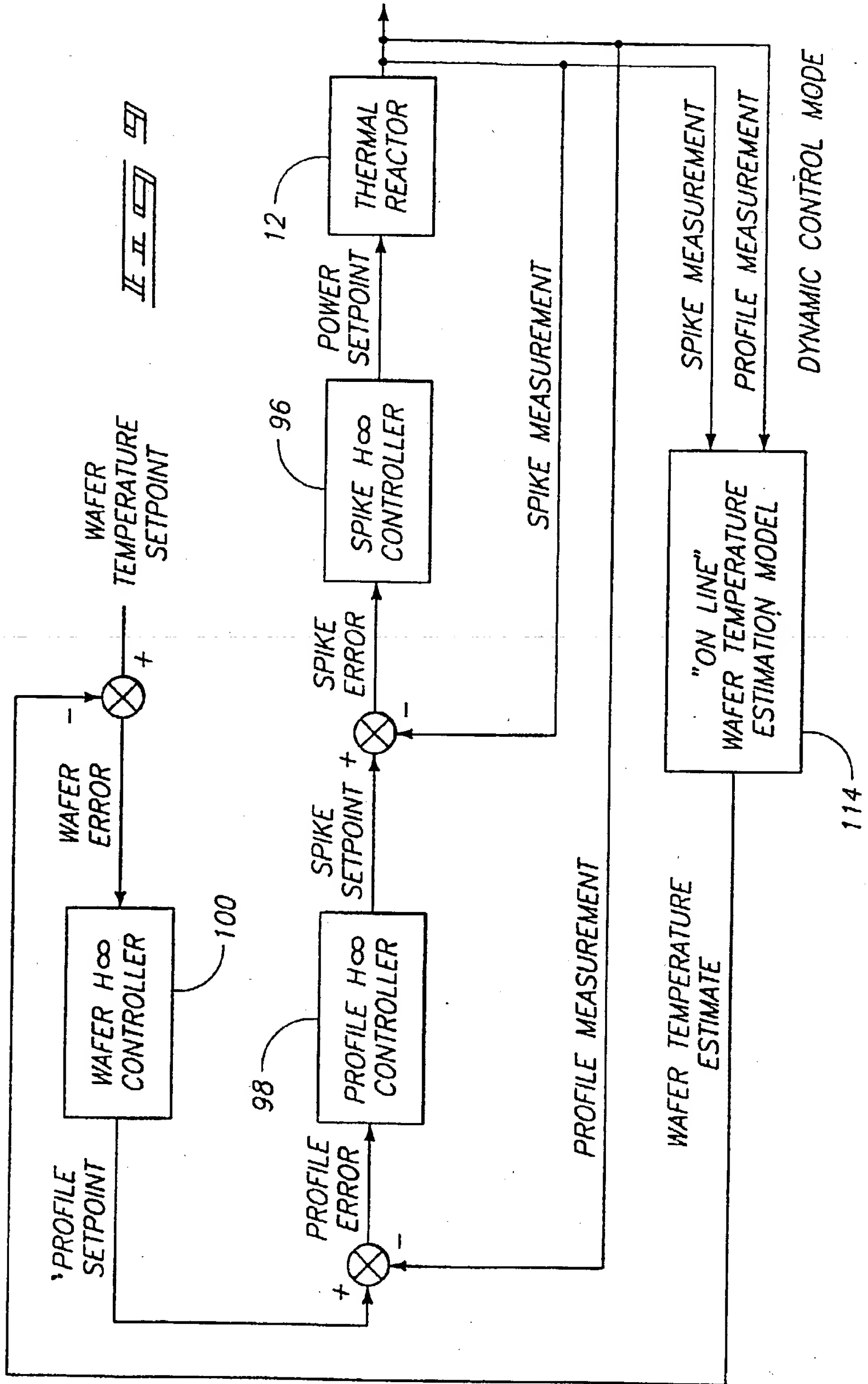


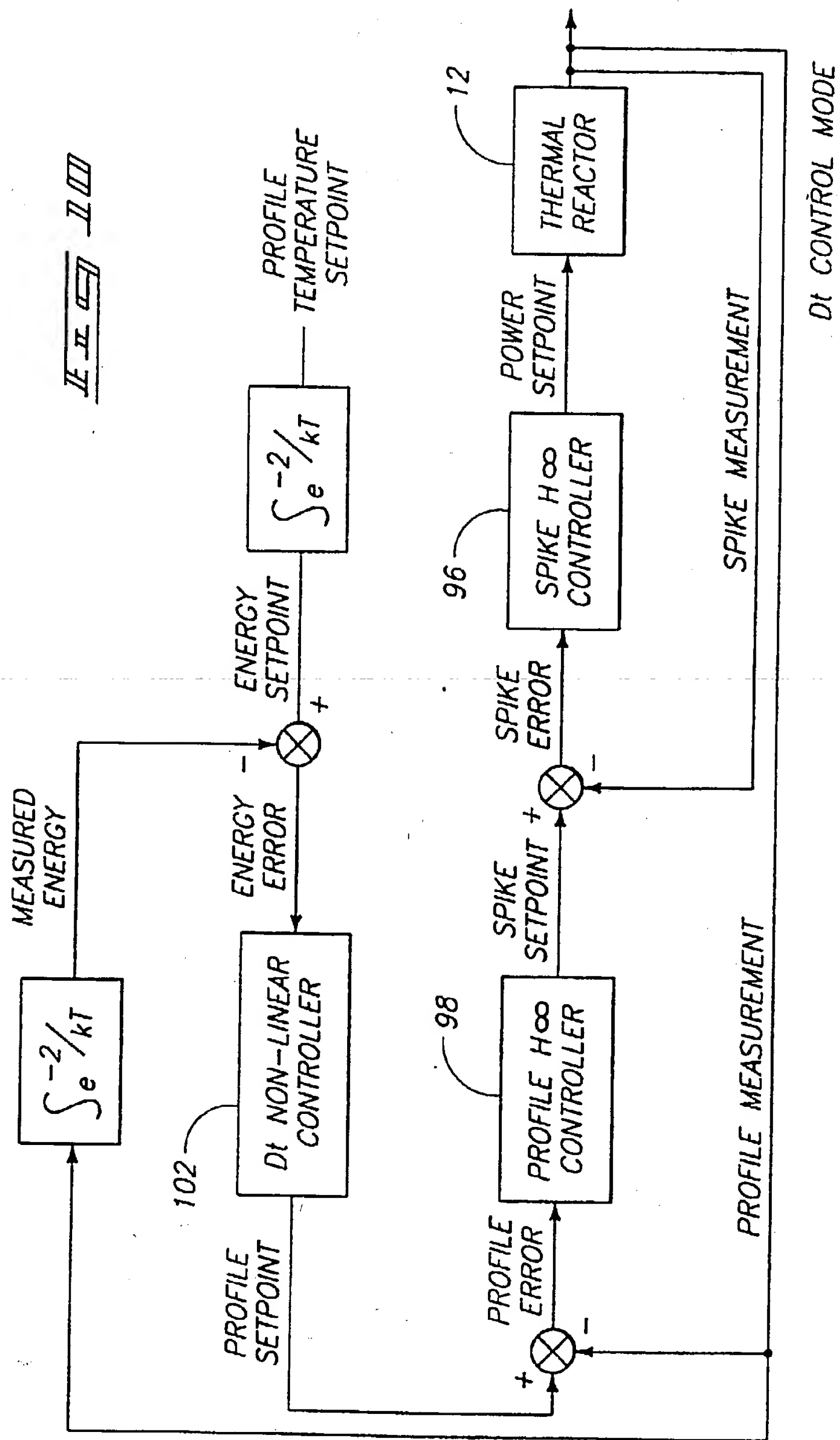
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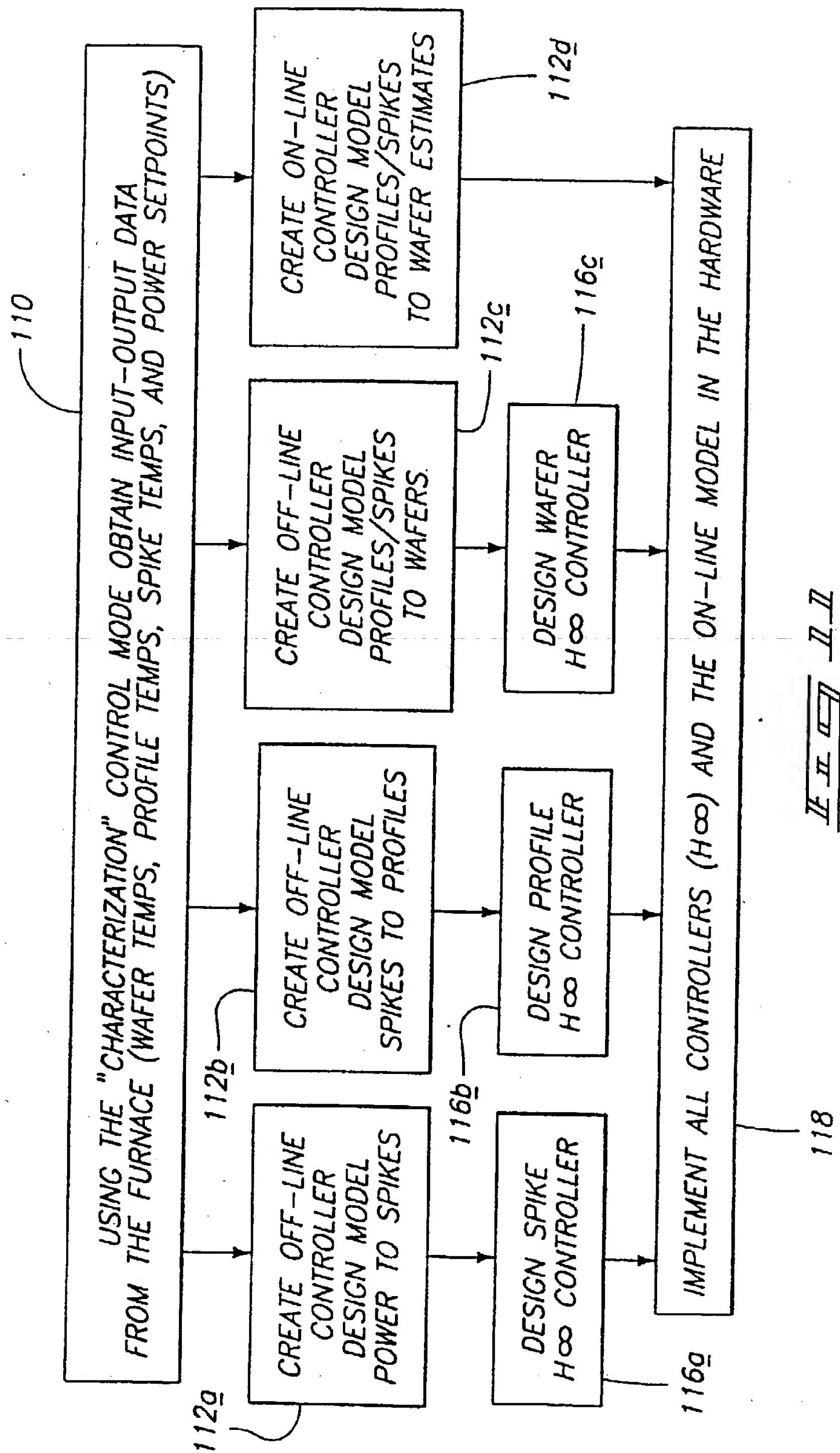


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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/01076

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H05B 1/02 ,C23C 1454

US CL :Please See Extra Sheet.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 392/416; 219/497,483,486;
118/725

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

156/345;
219/501,485, 494,505

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, Japanese Patent Abstracts

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,5,517,594 A (SHAH ET AL) 14 MAY 1996, SEE ENTIRE DOCUMENT.	1-39
Y	US 5,099,442 A (FURUTA et al) 24 March 1992, SEE ENTIRE DOCUMENT.	1-39
A	US 5,258,601 A (TAKANO) 02 NOVEMBER 1993 , SEE ENTIRE DOCUMENT.	1-39
A	US 4,937,434 A (NAKAO) 26 JUNE 1990, SEE ENTIRE DOCUMENT .	1-39
A	US 4,761,538 A (CHIBA ET AL) 02 AUGUST 1988, SEE ENTIRE DOCUMENT	1-39

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
A document defining the general state of the art which is not considered to be of particular relevance	*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
E earlier document published on or after the international filing date	*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*G* document member of the same patent family
O document referring to an oral disclosure, use, exhibition or other means	
P document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

06 APRIL 1998

Date of mailing of the international search report

07 JUL 1998

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/01076

A. CLASSIFICATION OF SUBJECT MATTER:

US CL :

392/416; 219/497,483,486;
118/725